

16

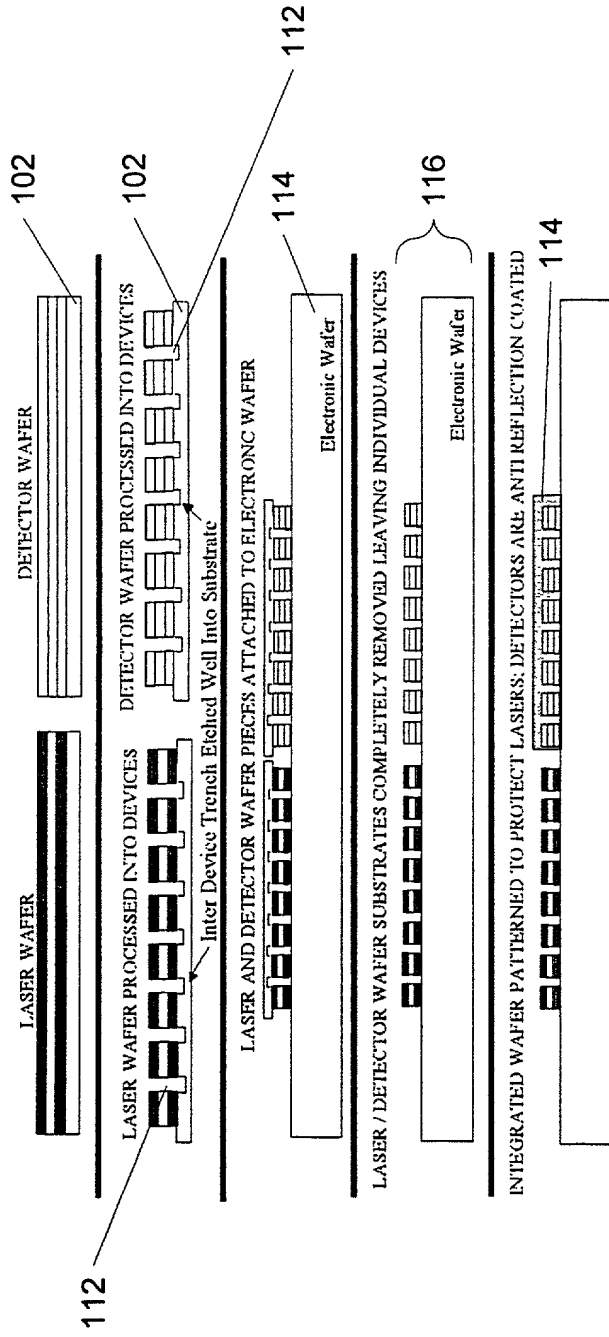


FIG. 2

FIG. 3

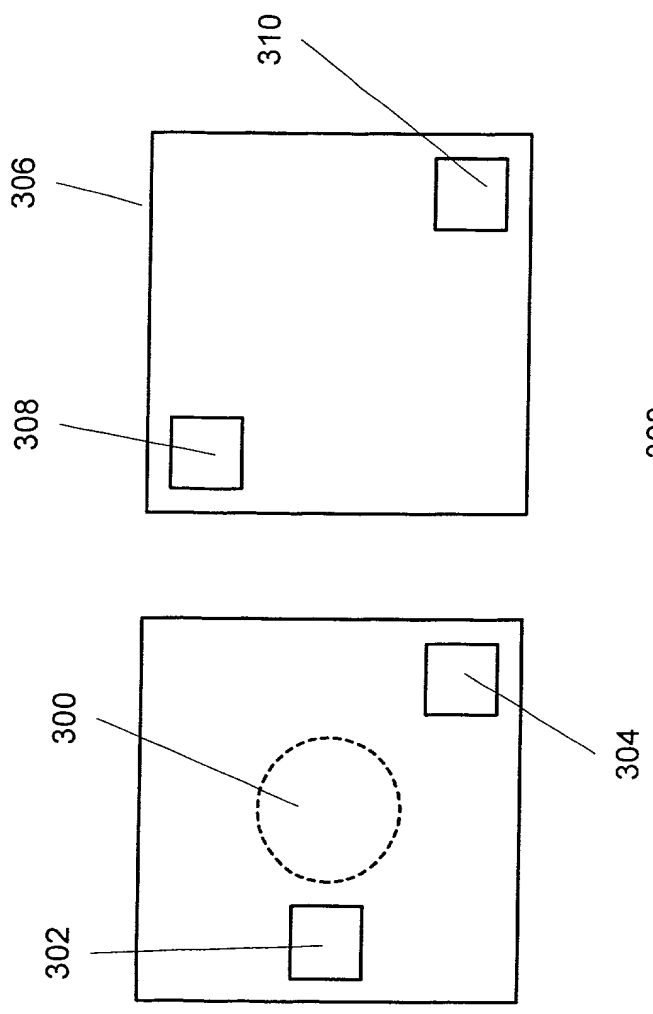


FIG. 3

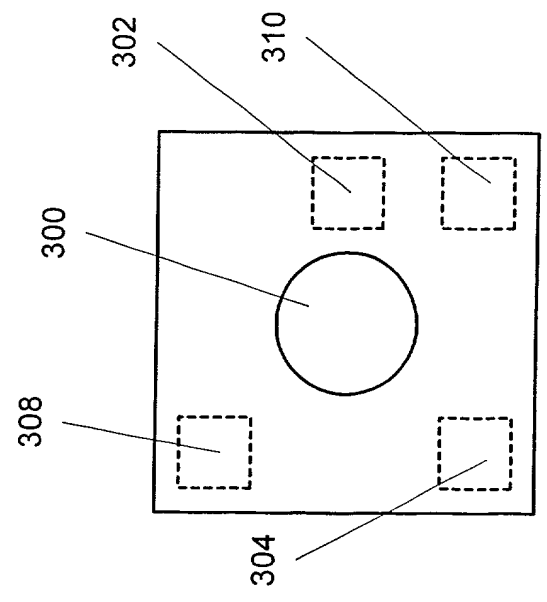


FIG. 4

FIG. 5 is a schematic diagram of a multi-layered structure 100, showing a cross-sectional view of the structure. The structure 100 includes a substrate 102, a first layer 104, a second layer 106, a third layer 108, a fourth layer 110, a fifth layer 112, a sixth layer 114, a seventh layer 116, and an eighth layer 118. The layers 104, 106, 108, 110, 112, 114, 116, and 118 are stacked on top of the substrate 102. The layers 104, 106, 108, 110, 112, 114, 116, and 118 are made of different materials, and the thickness of each layer is indicated by a dimension line and a label. The thickness of the substrate 102 is indicated by a dimension line and a label 't'.

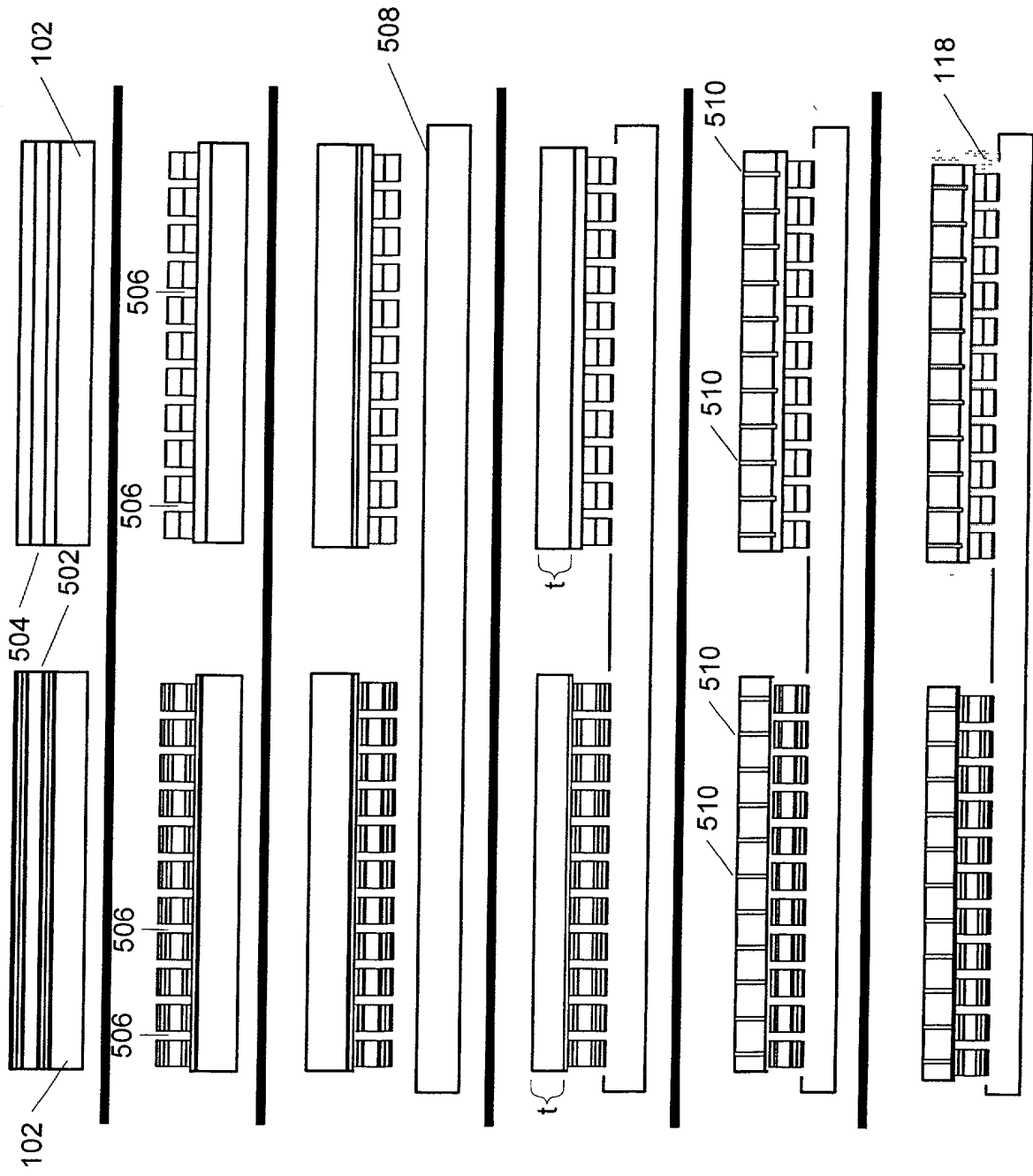


FIG. 5

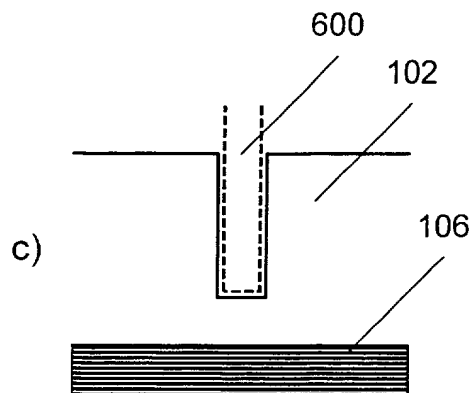
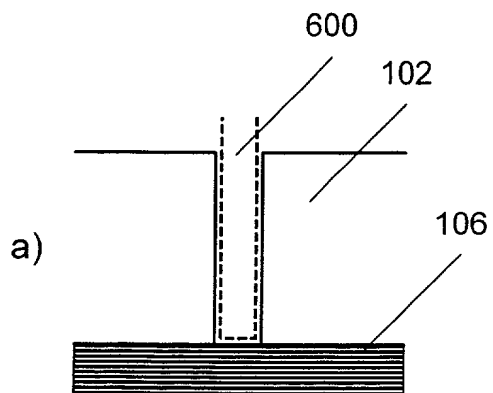
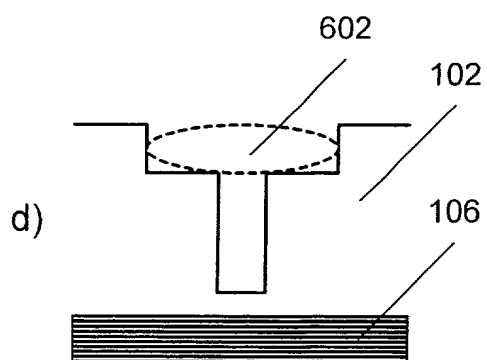
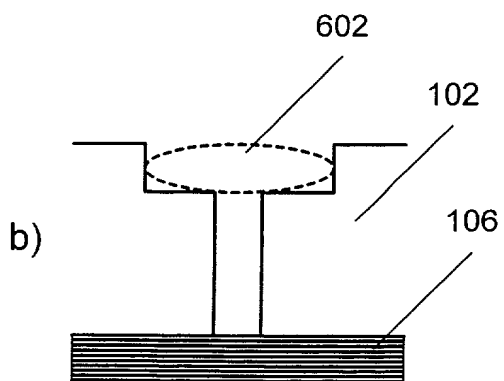


FIG. 6



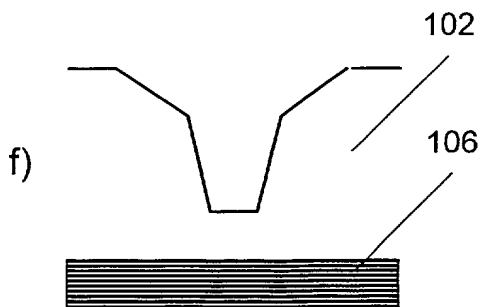
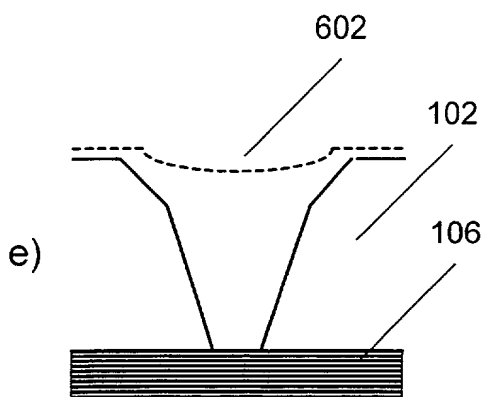
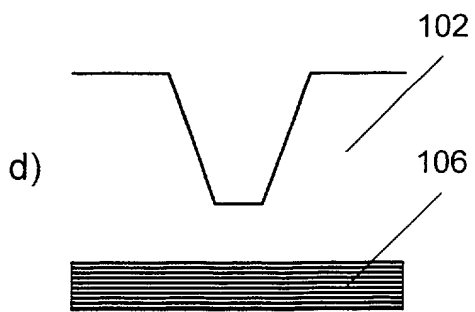
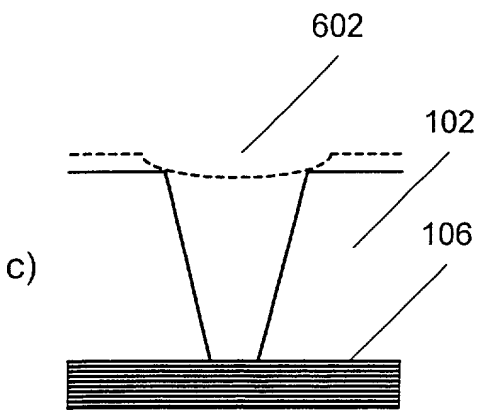
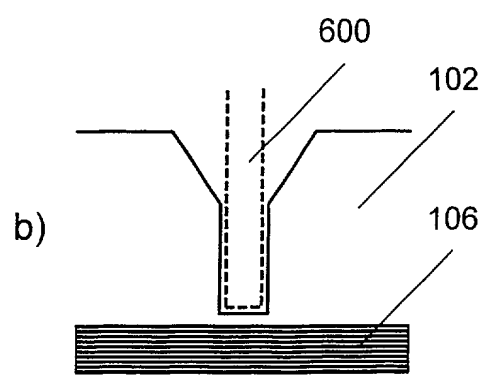
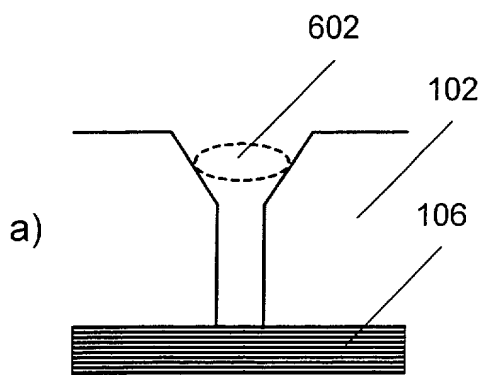


FIG. 7

FIG. 8 is a perspective view of a first embodiment of a device 600, showing a plurality of vertical rods 102 and a base 106.

FIG. 8

600

102

106

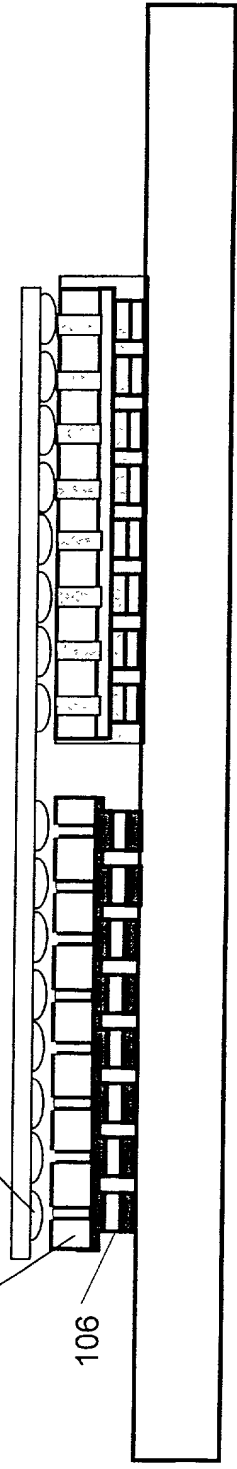


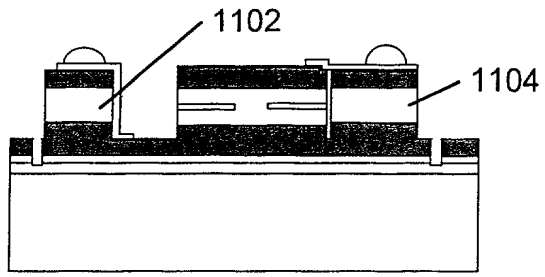
FIG. 9

602

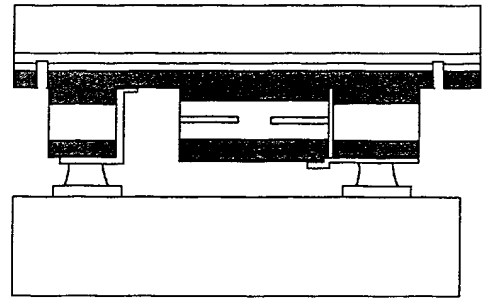
102

106

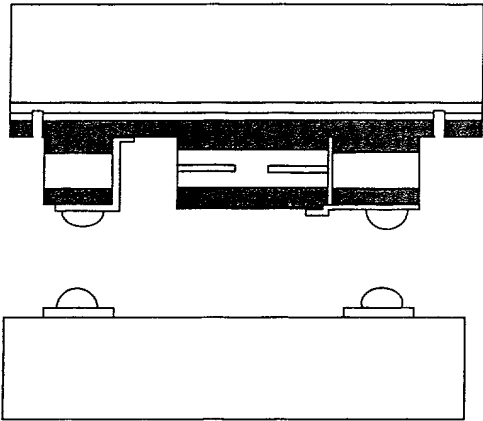




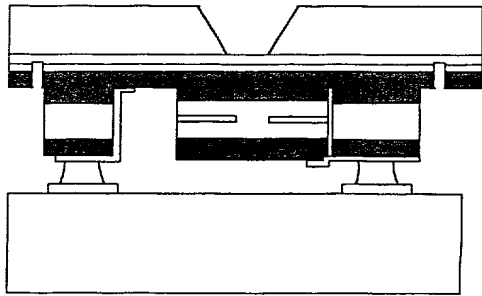
a)



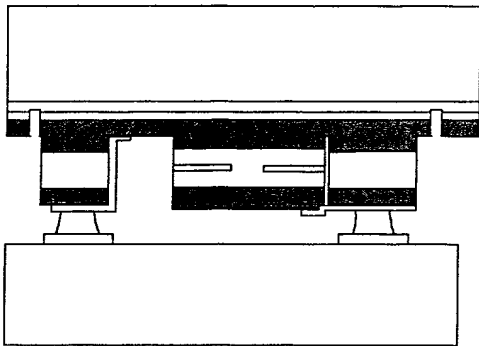
d)



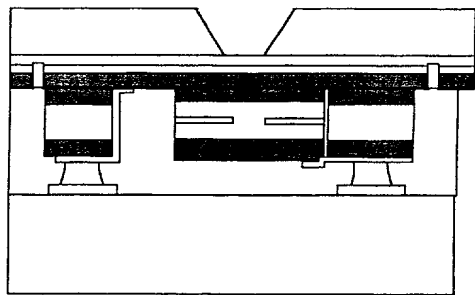
b)



e)



c)



f)

FIG. 11

FIG. 12

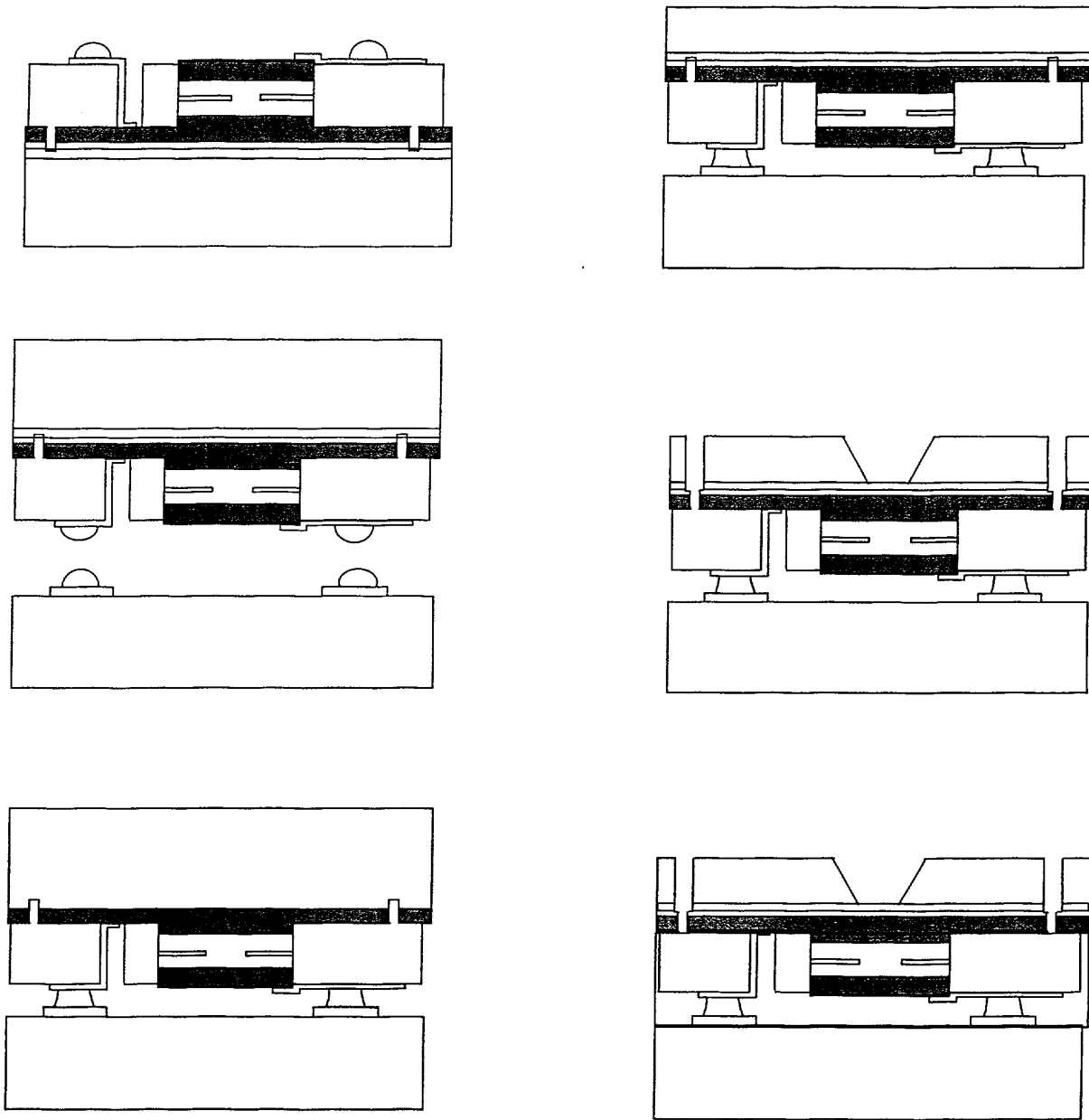


FIG. 12

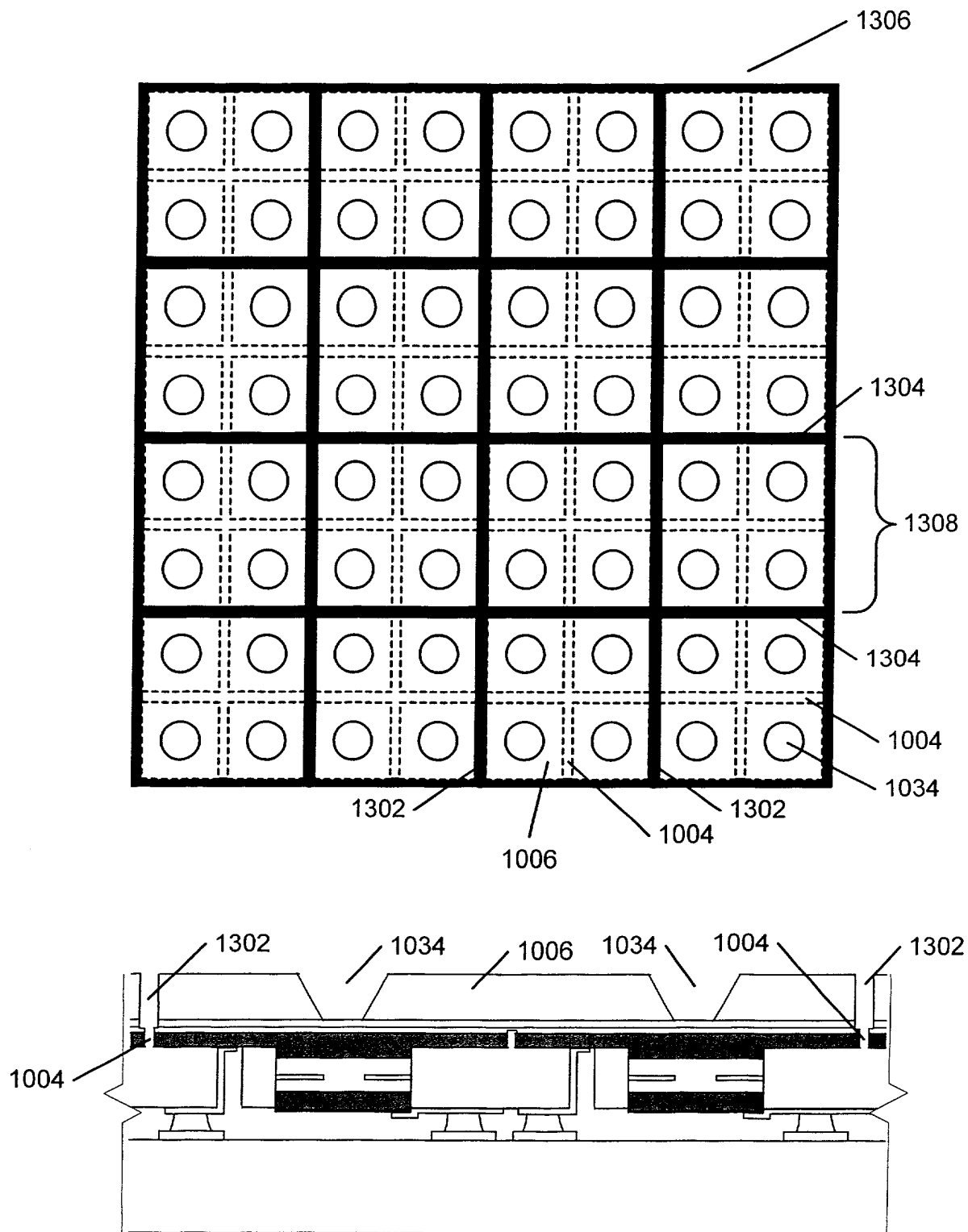
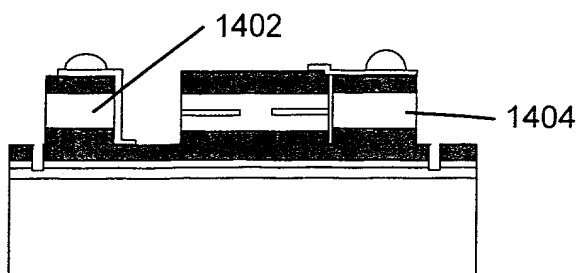
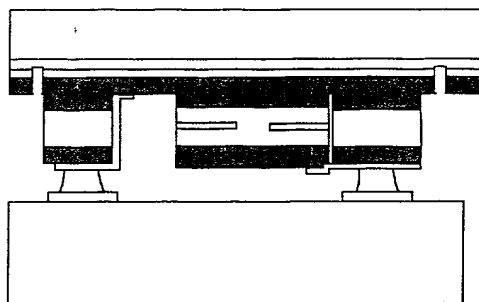


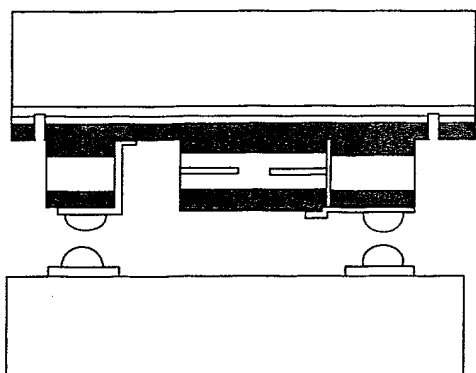
FIG. 13



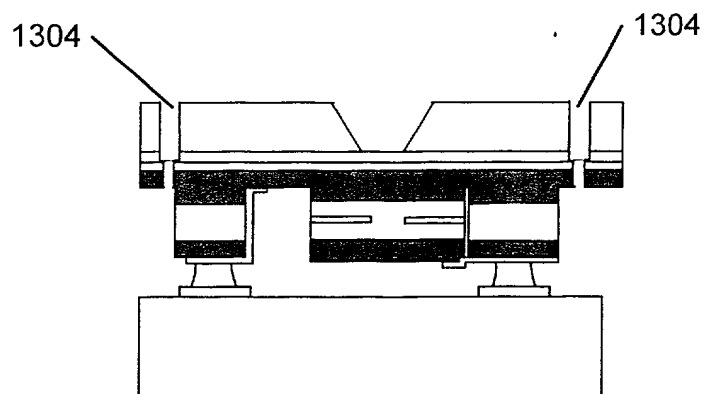
a)



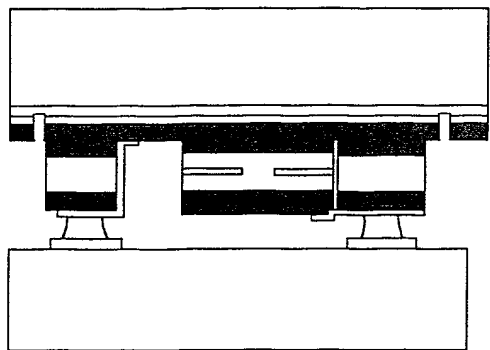
d)



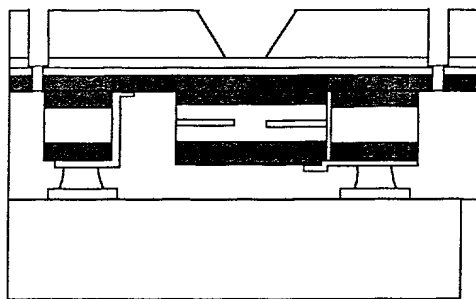
b)



e)



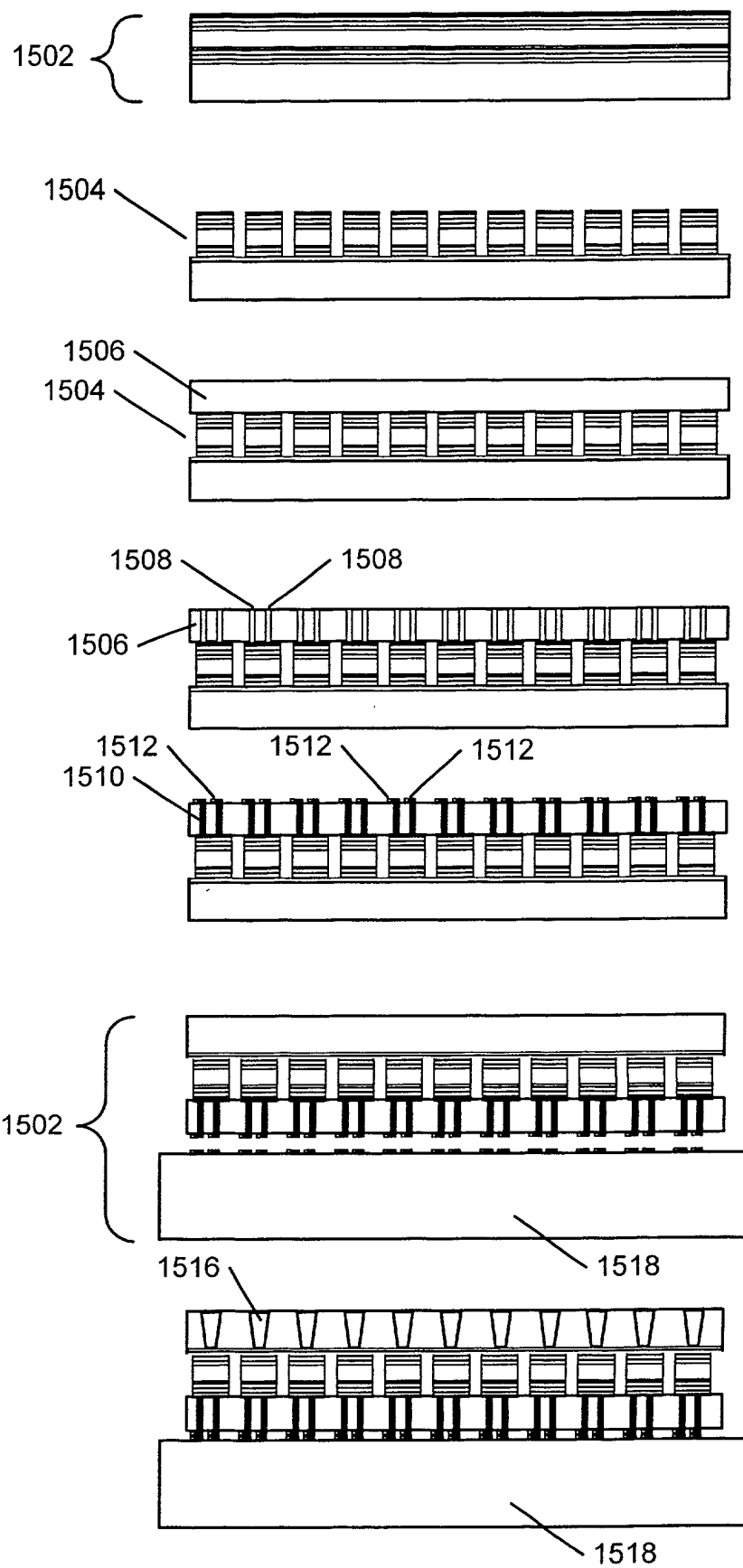
c)



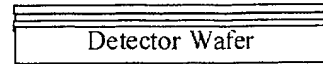
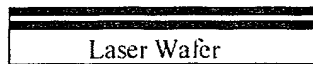
f)

FIG. 14

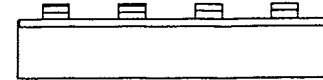
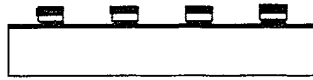
FIG. 15



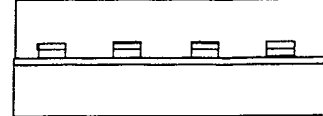
Optical wafers
(e.g Laser and
Detector wafers)



Process into
individual devices



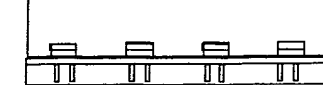
(Optional)
Attach carrier



Thin substrate
to appropriate
thickness to
facilitate etching



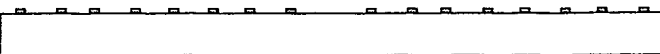
Etch vias (or drill
holes) and pattern
with insulator



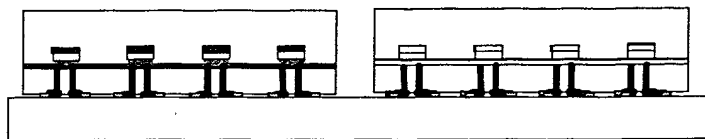
Fill vias or holes
with conductive
material



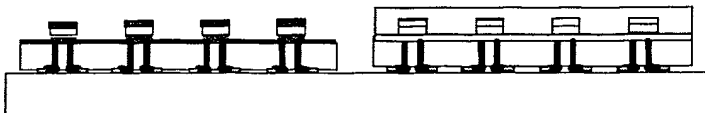
Pattern wafer
substrate to match
pad locations on
electronic chip



Attach optical
chip to electronic
chip using now
matching pad
locations



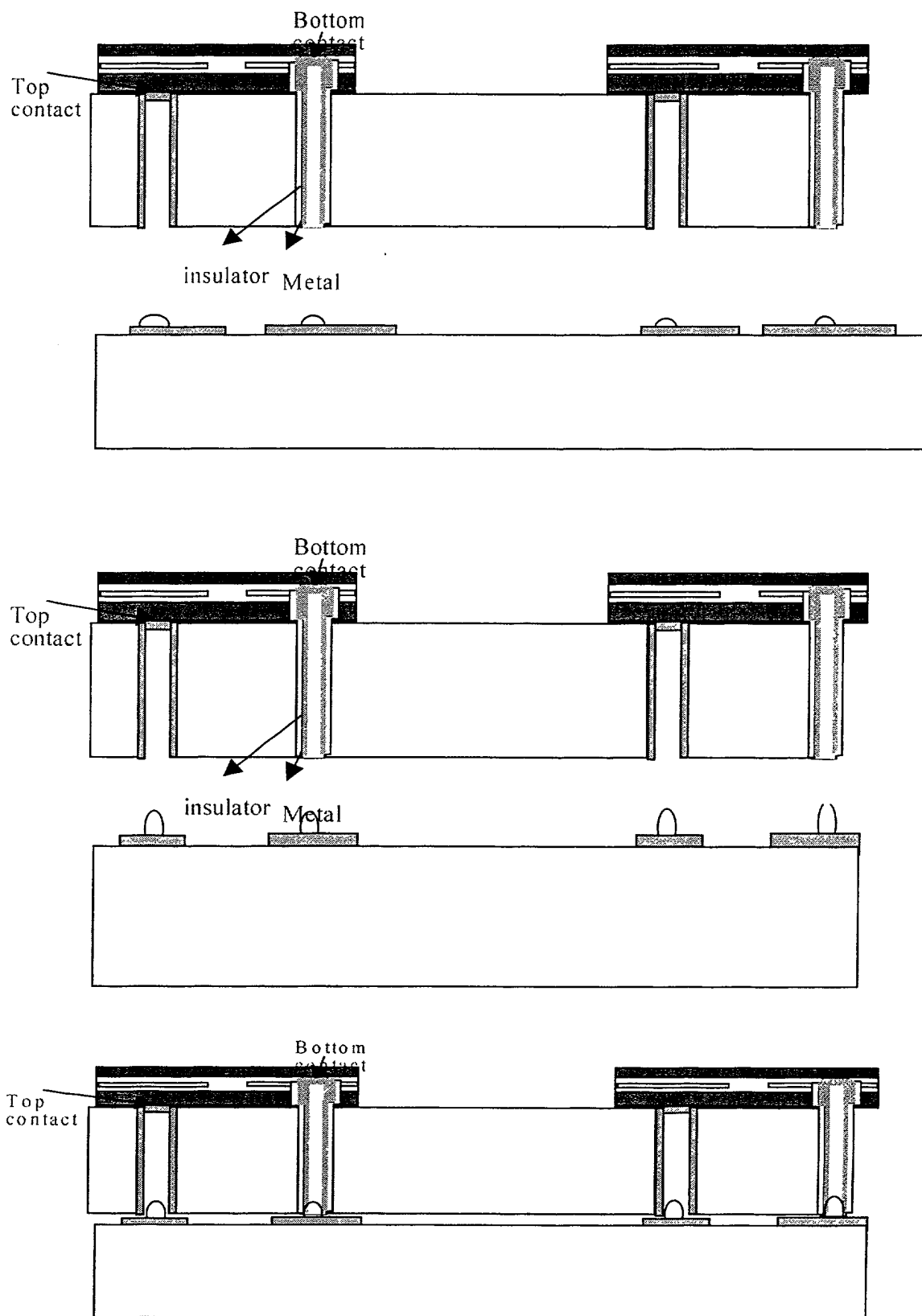
(Optional)
Remove holder



(Optional) AR
coat detectors

FIG. 16A

FIG. 16B



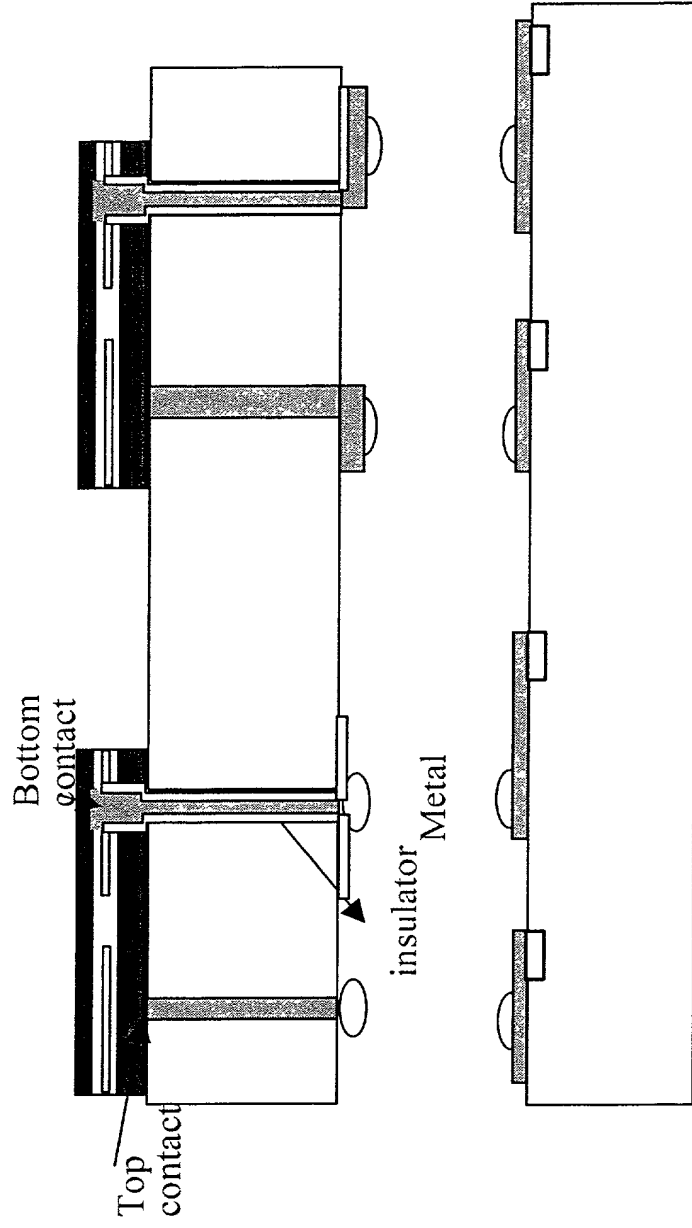


FIG. 16C

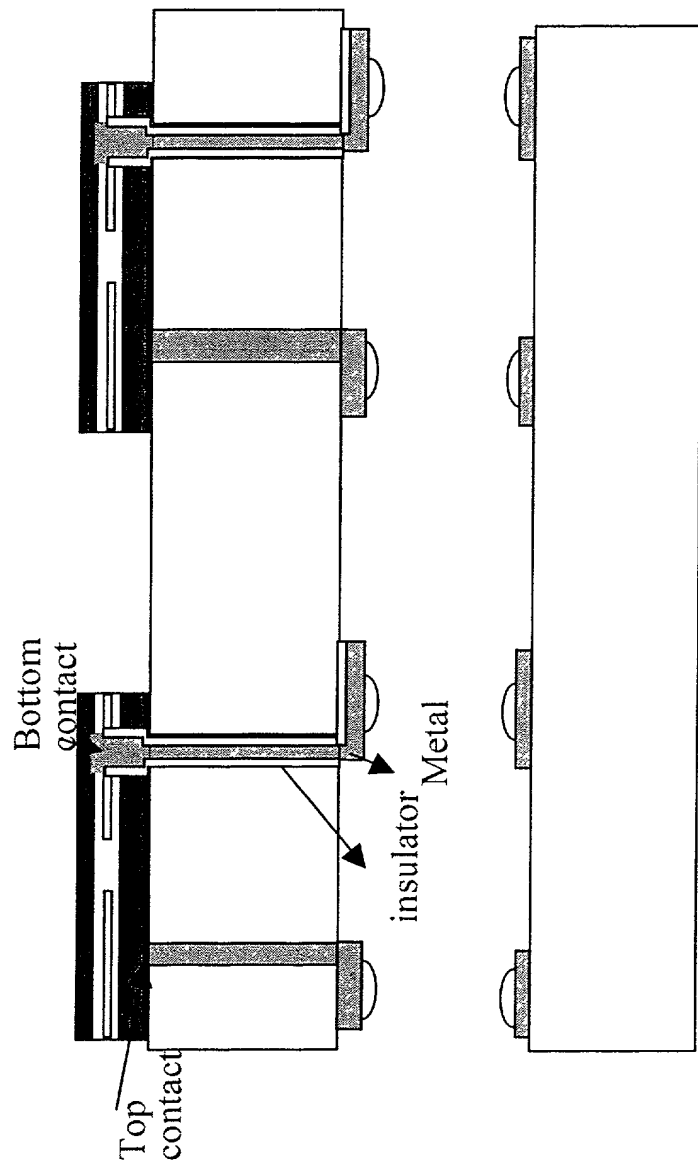


FIG. 16D

FIG. 17

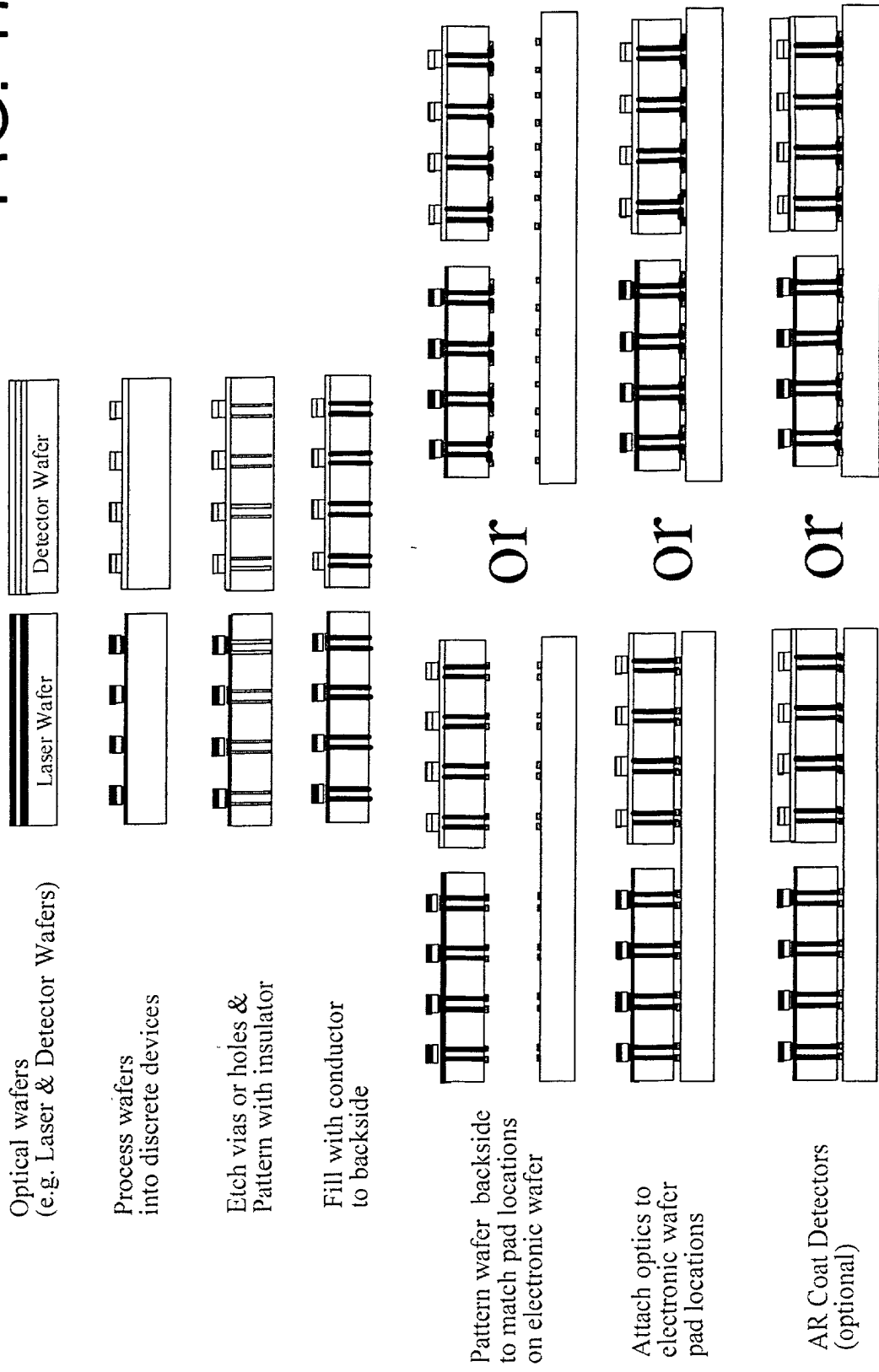


FIG. 18 is a schematic diagram of a device 1800, showing a top view and a bottom view. The top view shows a rectangular frame 1802 with a central L-shaped component 1806. The L-shaped component 1806 has a horizontal arm 1812 and a vertical arm 1814. The horizontal arm 1812 has a circular feature 1818 at its end. The vertical arm 1814 has a circular feature 1816 at its end. The bottom view shows the same rectangular frame 1802, but the L-shaped component 1806 is shown in a different orientation. The horizontal arm 1812 is now vertical, and the vertical arm 1814 is now horizontal. The circular features 1818 and 1816 are still present. The bottom view also shows a dashed rectangular area 1808 in the upper left corner and a dashed rectangular area 1810 in the lower right corner. The text "(SEE THROUGH)" is written vertically next to the bottom view.

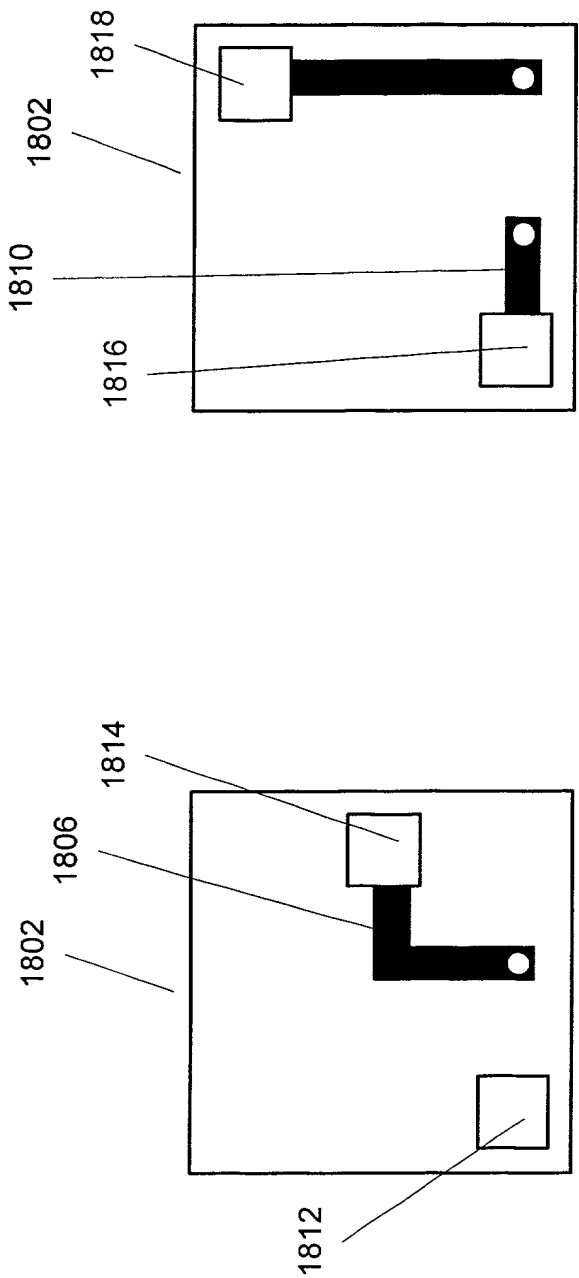
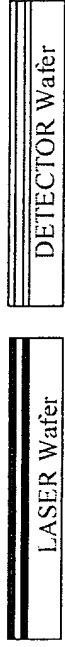


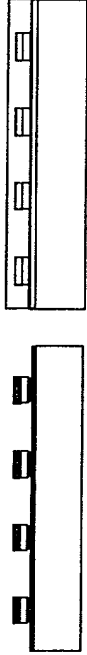
FIG. 18

Optical wafers

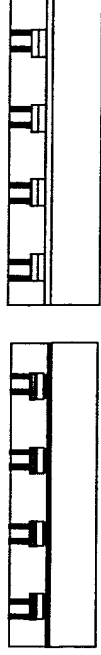
(e.g Laser & Detector wafers)



Process into individual devices
& AR coat detectors



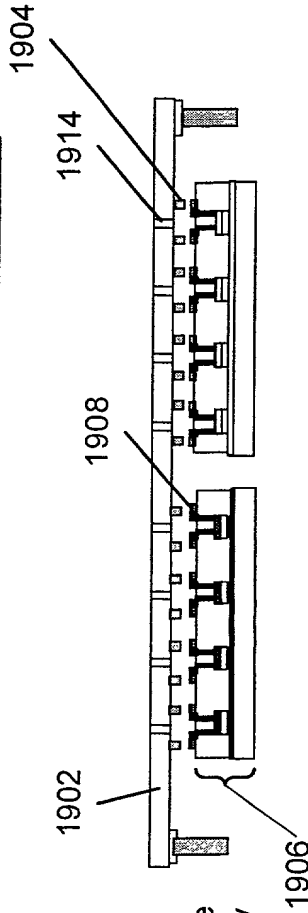
Cover devices with insulator and
pattern vias through to device
contact pads



Pattern optical device wafer
to create traces to locations
that will match mating
contacts on adapter



Attach optical device chip
to adapter via aligning
pads created by patterning
(NOTE: Holes in adapter can be
created pre-post or concurrently
with wafer patterning



Integrate adapter chip with
electronic chip via standoffs,
wires, etc.

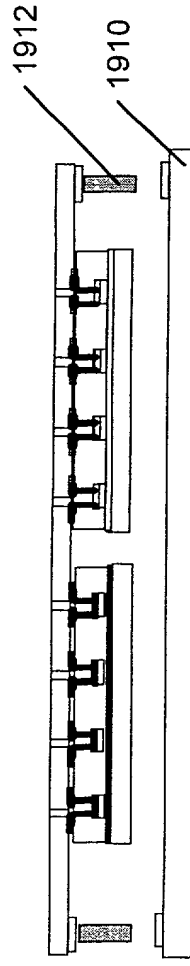


FIG. 19

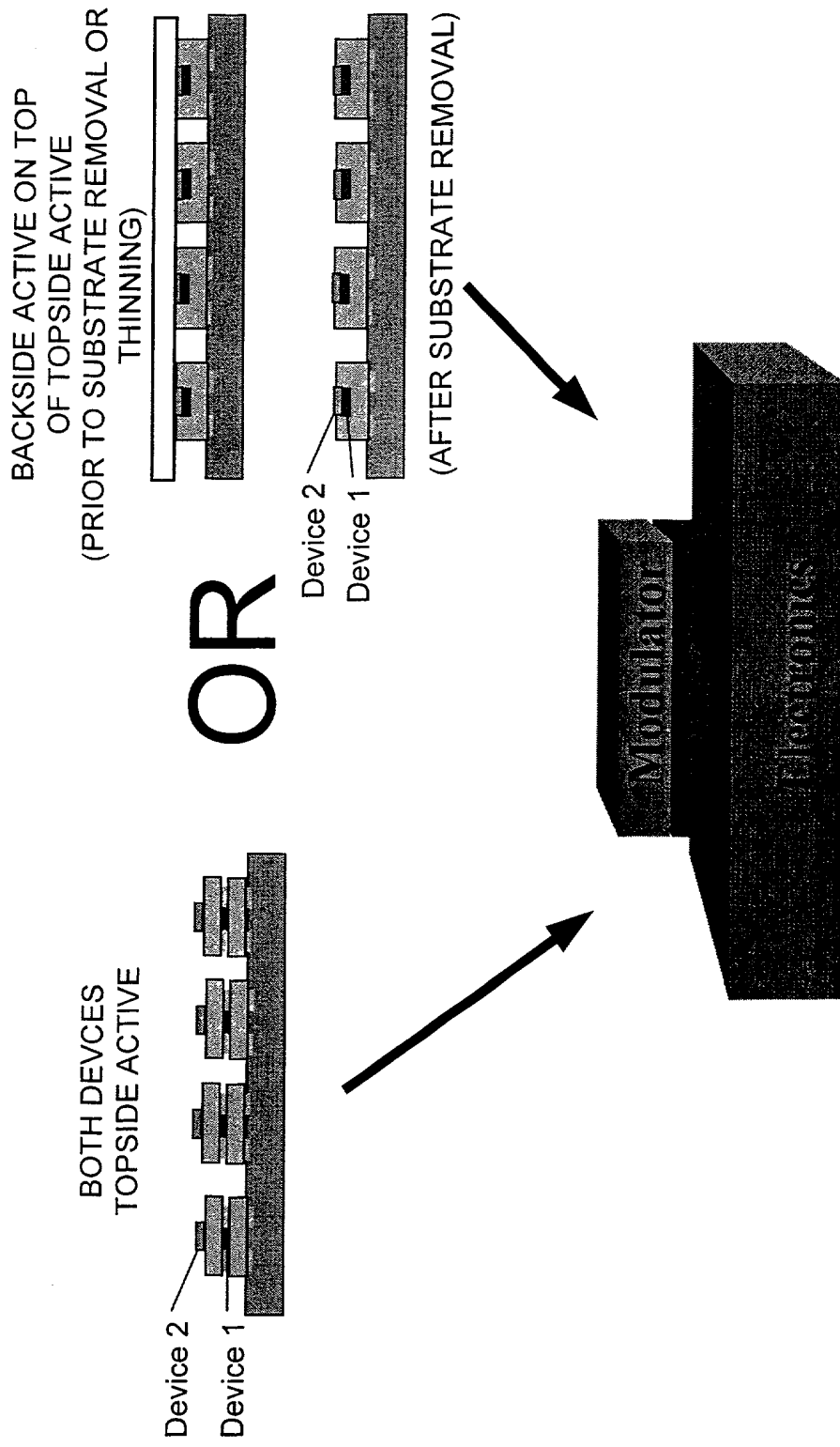


FIG. 20A

40 Gb/s = 20 GHz = 50ps
Wavelength in free space = $3 \times 10^{10} \text{ cm/s} \times 50^{12} \text{ s} = 1.5 \text{ cm}$
1/8 wavelength in $n=3 = 640 \text{ microns}$

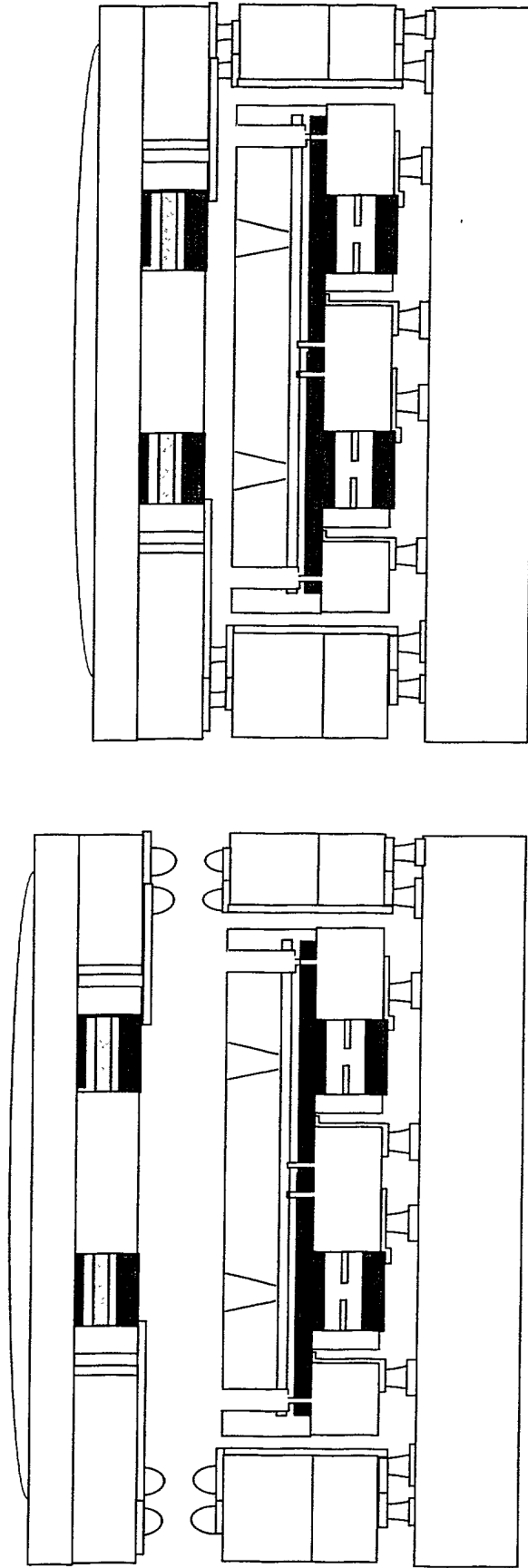


FIG. 20B

FIG. 21

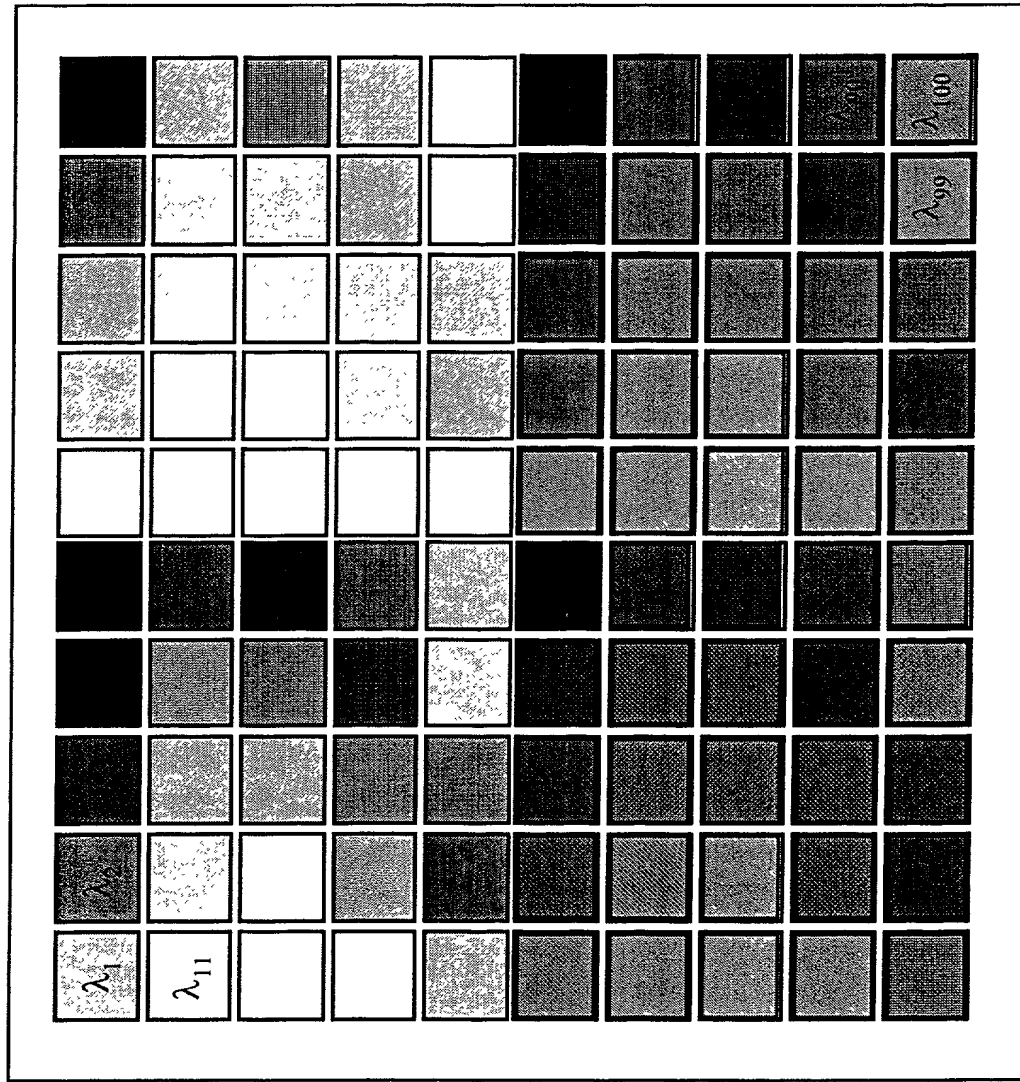


FIG. 21

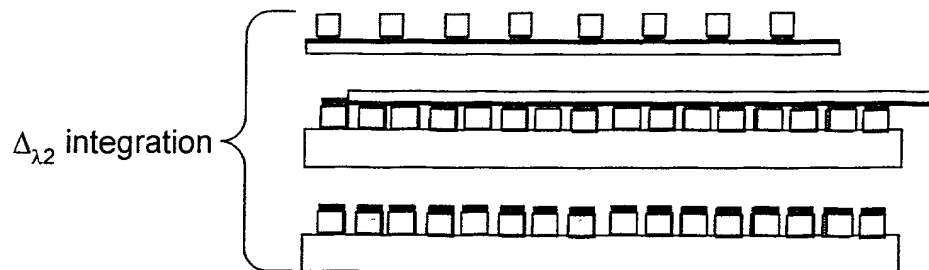
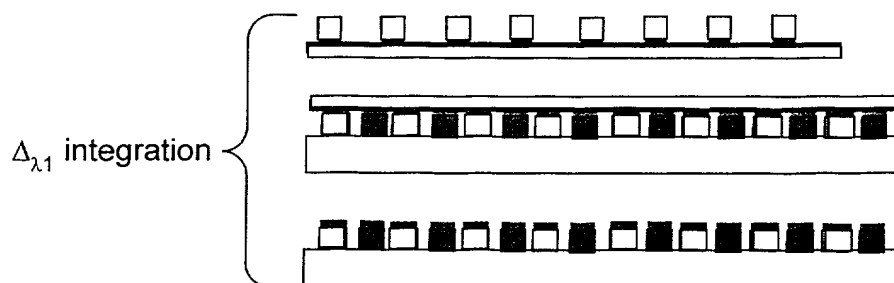
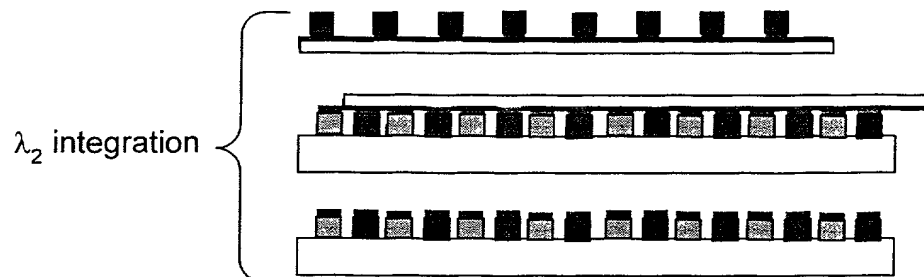
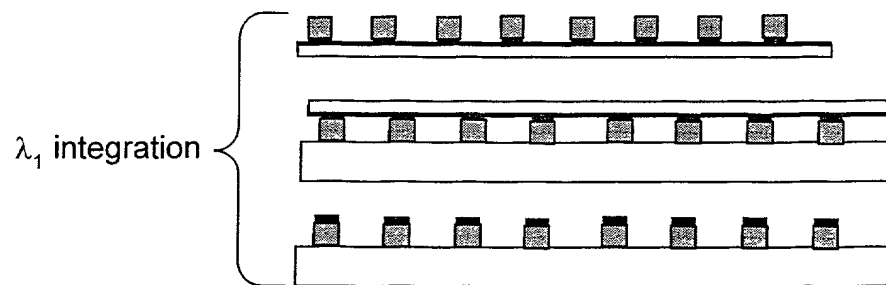
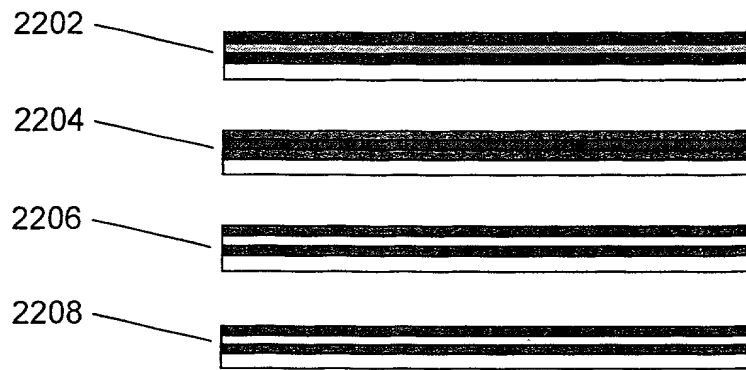


FIG. 22

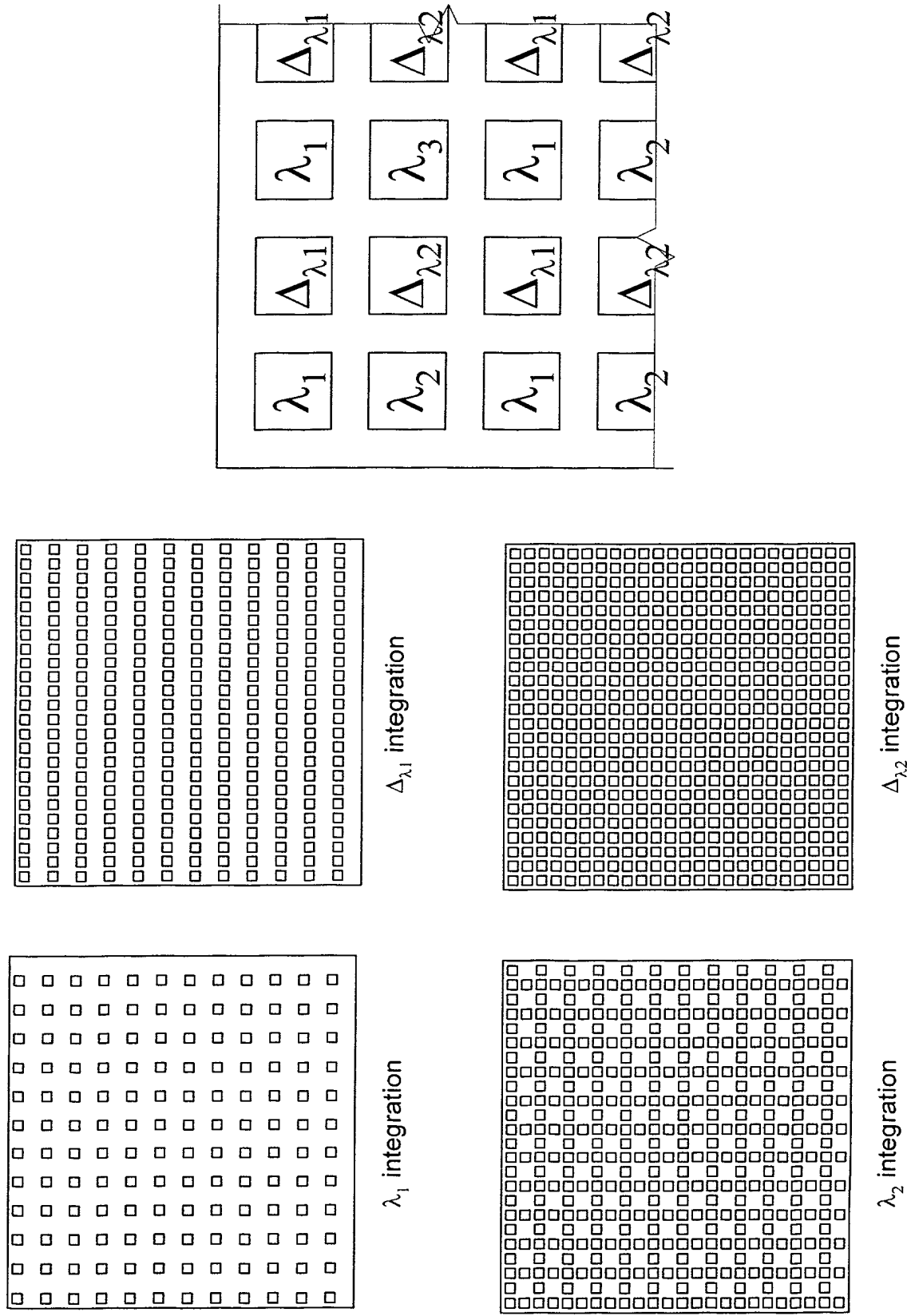


FIG. 23